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KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
RAO, G NAGESH	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/799,335
Filing Date: March 12, 2004
Appellant(s): TOMASINI ET AL.

Kyle F. Schlueter
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6/11/07 appealing from the Office action mailed 11/01/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US 2003/0157787 Murthy et. al. 08-2003

Mayer, J. and Lau, S.S., "Electronic Materials Science: For Integrated Circuits in Si and GaAs", P. 40.

Applicant's Admitted Prior Art (Page 6 Section 0019 of the Specification).

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

ISSUE 1

Claims 1-4, 6, 9-15, 19, 21-28, 31-32, 34, 39-45, and 51-53 are rejected under 35 U.S.C. 102(e) as being anticipated by Murthy (US PG Pub 2003/0157787).

Examiner would like to point out that the claims filed by applicant are understood to be a mixture of process and product by process claims. Therefore the application will be treated on these merits when applicable.

Murthy 787 teaches a method including the blanket deposition of a SiGe film comprising of the intermixing of a silicon (Si) source, a germanium (Ge) source, and an etchant to form a gaseous precursor mixture under a CVD process, whereby the layering can occur as a blanket layer of the sorts. Examiner points out that in figure 5 as understood by the process diagram, the process begins with loading a wafer (i.e. substrate) into a CVD chamber, followed by introducing the Si source gas such as silane into the CVD chamber as well the etchant source gas such as HCl (etchant gas source flow continues throughout the deposition process), and then decreasing the flow of Si flow while introducing the Ge gas source such as germane, thereby having an intermixing of all three gas sources simultaneously, and as can be explicitly shown for example in Figure 2 there is a Si Substrate (202), a buffer layer of SiGe (204), and a Ge or other film layer of the sorts (206) deposited over the buffer layer of SiGe which reads on as an epitaxial blanket layer deposited over the substrate which may be a monocrystalline semiconductor wafer (See Sections 0021-0026 and 0029, as well Figures 1-9D).

Furthermore in another embodiment of Murthy 787 it is understood by the Figure 5 flow process diagram that a substrate can be placed in the CVD chamber for pre-processing where a dielectric mask (reading on dielectric material) such as SiO_2 a known type of oxide material, is positioned over the substrate and the brief

introduction of Si source gas such as silane, and HCl (a commonly known type of etchant in semiconductor processing) therefore creating an initial pattern of the sort such as a shallow treanch isolation scheme as can be seen in figure 9a or 4b before the forming of the SiGe buffer layer over the patterned substrate and thereafter any other deposited film layers over the SiGe buffer layer and the patterned layer over the substrate which would read on as a type of underlying blanket layer (See Sections 0028-0034).

Furthermore Murthy 787 teach various flow rates of the silicon, germanium, and etchant flow gas sources. These flow rates in their own right help determine the mass amount of the material presented into the CVD chamber system, as so described by applicant's specification on page 6. Therefore based on that statement, it is understood that the flow rates taught in Murthy 787 can be altered to achieve a mass amount where the combined Si and Ge gas sources weigh more than the etchant gas source. For example the flow of Si and Ge sources range from 0-200 sccm and 0-500 sccm respectively, whereas the HCl source flows in at about 50 sccm (which falls between the prescribed 1-200 and 25-50 sccm ranges for the etchant) (see Sections 0029-0030 and 0035-0042).

Finally the temperature ranges for the CVD process range from 625-700^0 C which fall within the range prescribed by applicant's claim of 350-1100^{0}C, and the pressure of the chamber is at 1 atm which is the equivalent of 760 torr.

ISSUE 2

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murthy (US PG Pub 2003/0157787) in view of Mayer, J. and Lau, S.S. **Electronic Materials Science: For Integrated Circuits in Si andGaAs,** P. 40.

From the aforementioned Murthy 787 teaches a process for depositing SiGe buffer layer on a substrate. This process includes teaching the use of a dielectric material mask, in Murthy 787's case the use of SiO_2 a well known gate dielectric oxide. However Murthy 787 failed to teach an alternative well known gate dielectric nitride.

In a literature reference pertaining to electronic materials processing, Mayer and Lau teach that oxides and nitrides are equivalents in the gate dielectric field.

Therefore at the time of the invention it would have been obvious to one having ordinary skill in the art to modify the teachings of Murthy 787 with that of Mayer and Lau, to realize that using a nitride in lieu of oxide as the dielectric material as a substitution of equivalents.

ISSUE 3

Claims 7-8, 16-18, 29-30, 33, 35-38, and 46-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murthy (US PG Pub 2003/0157787) in view of applicant's admitted statements of prior known states of the art via routine experimentation on page 6 of the specification.

From the aforementioned Murthy 787 teaches a process for depositing SiGe buffer layer on a substrate. This process includes teaching the use of varying deposition, gas flow source, etchant source, CVD, temperature, and pressure variation standards. As admitted by applicant these processes utilized to obtain specified surface roughness values and conditions imposed on the system are the result of routine experimentation.

Therefore it would be obvious to one having ordinary skill in the art at the time of the invention to implement varying conditions as set forth by the system and process taught by Murthy 787 to include routine experimentation in order to optimize the process and system. Through optimization of these procedures allows for better control and better product quality when fabricating the SiGe film layer. It is also understood and well known that these product characteristics are directly related to pressure, temperature, and material flow parameters, and therefore

further substantiates that these claims would be obvious in light of routine experimentation to achieve desired results.

(10) Response to Argument

ISSUE 1

Applicant's arguments filed 6/11/07 have been fully considered but they are not persuasive. Examiner respectfully disagrees with applicant's response that Murthy 787 does not anticipate the prior art.. Murthy 787 clearly taught (for example in Figure 5) the method for blanket depositing of a SiGe film comprising the intermixing of a Si source, Ge source, and an etchant to form a gaseous precursor mixture, flowing the gaseous precursor mixture over a substrate under CVD and depositing a blanket layer of epitaxial SiGe over the substrate formed in part from the gaseous premixture (See Sections 0021-0030 and 0035-0042). Applicants instead focused on one particular portion of an embodiment taught but never took the whole reference and steps layed out in its fullest form as taught and shown in the rejections based on the prior art. Just because Murthy 787 in one instance teaches selective deposition does not preclude it from being a form of blanket deposition. The same method of Murthy 787 is applied as applicant's claimed invention, and if there is something different from the end result, it is due

to something that applicant's are not claiming, because the language is read on by Murthy 787.

ISSUE 2

Applicant's contend that examiner is mixing various embodiments to meet applicant's preferred claim language and imply that examiner has erroneously applied an USC 102(e) rejection because of the single reference in contrast to a USC 103(a) rejection. Examiner disagrees with this assertion, because as clearly pointed out from the beginning of the first non-final office action, examiner pointed to Figure 5 as a clear example of how applicant's invention was read on by the prior art. It was via a phone discussion that applicant's inquired with examiner about the rejection and began arguing about "the combination" of alternative embodiments, which examiner rebutted but doing so in response to the nature of their arguments and not to the extent of applying the prior art.

Applicant's contend that Murthy 787's deficiency is that it teaches blanket deposition without the use of an etchant material (i.e. HCl), which is an incorrect assertion. Murthy 787 clearly teaches the blanket deposition of the SiGe layer on the substrate during the course of the whole time use of HCl etchant gas source. Selective deposition as denoted before constitutes as a form of blanket deposition,

there is nothing precluding it from being one, especially as denoted by applicant's claimed language.

ISSUE 3

Applicant's provided no rebuttal towards the USC 103 (a) rejection, except that Murthy 787 was not viable prior art and that Mayer et al. reference did not cure said "deficiencies". However Mayer et al was utilized to teach nitrides and oxides were viewed as substitution of equivalents, an argument applicant's never contended, therefore it is the examiner's position that this rejection is viable and appropriately applied.

ISSUE 4

Applicant's provided no rebuttal towards the USC 103 (a) rejection, except that Murthy 787 was not viable prior art and that examiner's position of page 6 Section 0019 was not admitted prior art. However examiner has noted that applicant's provided no rebuttal just noting that it did not cure Murthy 787's deficiencies as based on primary reference and nothing more. Examiner asserts that section 0019 denotes the paragraph description with "routine experimentation", leading examiner to believe that it is viable prior art and appropriately applied for the USC 103 (a) rejection utilized by examiner. There being no remarks against

what was specifically applied by examiner for the rejection, it is the examiner's opinion that the rejection was appropriate and viable.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

7/19/07

GNR (G. Nagesh Rao)

DUANE SMITH
PRIMARY EXAMINER

7-20-07

Conferees:

/Jennifer Michener/

Quality Assurance Specialist, TC1700

Jennifer Kolb Michener

Duane Smith